A "Probe-Lift" MOS-Capacitor Technique for Measuring Very Low Oxide Leakage Currents and Their Effect on Generation Lifetime Extraction

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***Abstract*—A new method for precisely measuring low gate oxide currents by measuring the charge leaking through the oxide in a pulsed metal oxide semiconductor capacitor (MOS-C) is presented. Using basic equipment, it is possible to measure currents less than $10\ \mathrm{fA/cm^2}$. The relevant theory is developed to use these capacitance–time data to extract an approximate leakage current and the effect on the extracted generation lifetime. The technique is simple and requires the same equipment used for pulsed MOS-C generation lifetime measurements. Experimental results are presented, which are consistent with theory.**

***Index Terms*—Leakage currents, MOS capacitors, semiconductor device measurements, semiconductor device reliability, silicon compounds.**

I. Introduction

SINCE suggested by Zerbst in 1966, the pulsed metal oxide semiconductor capacitor (MOS-C) technique of lifetime measurement has become a common method of characterizing the generation lifetime in semiconductors [1]. Many similar techniques have been devised [2], [3], and interpretation of the data has been carefully analyzed [4]. A thorough review of the relevant concepts and equations involved in this technique is given in Kang and Schroder [5]. The pulsed MOS-C technique offers several advantages: it uses a common test structure, the measurement region is controlled very precisely, and very short lifetimes can be measured.

However, a significant disadvantage is the presence of oxide leakage currents, which delay or prevent inversion layer formation, depending on the severity of the leakage current. In the following treatment, we propose a very simple addition to the pulsed MOS-C method, which allows the determination of the oxide leakage currents, enabling one to judge the accuracy of the lifetimes determined from the pulsed MOS-C data. We then develop a general model to explain the effect that leakage current has on the pulsed MOS-C method and the resulting analysis for various forms of leakage current. Finally, we present our experimental work, which is consistent with our analysis.

Several related "floating-gate" current measurement techniques have been developed and successfully implemented [6]–[9]. The most significant difference between our method and previous ones is that our method only requires a MOS-C, not a MOSFET. This is convenient, as often it is undesirable to fabricate a transistor to measure oxide leakage. Furthermore, our method is, in principle, similar to charge leaking from a floating gate in floating gate memories [electrically erasable programmable read-only memory (EEPROMs) and Flash]. A similar floating gate technique was also used to estimate the retention time of the inversion layer in a 4H-SiC MOS-C in order to demonstrate its potential as a nonvolatile memory [10].

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II. Theory

The theory of the pulsed MOS-C technique is detailed in [5], and is only briefly reviewed here. The procedure begins by pulsing the device from accumulation into deep depletion. Thermal generation causes the device to generate electron–hole pairs, which form an inversion layer and restore equilibrium. During this transitional period, the width of the space charge region (scr) continually decreases, resulting in a proportional increase in capacitance. This capacitance transient is recorded as a function of time and then used to create a Zerbst plot, which represents the generation current versus the scr width. The slope of this plot is proportional to the effective generation lifetime $\tau_{g,\mathrm{eff}}$, and the intercept is proportional to the effective surface generation velocity, $s_{g,\mathrm{eff}}$.

If a gate oxide leakage current is present, the interpretation of the measurement results and the resulting Zerbst plot become unclear. The oxide leakage current now drains the inversion layer that the generation current is trying to form. Clearly, this extends the recovery time, which increases the calculated lifetimes. For this reason, it important to know the gate leakage current if the results of the pulsed MOS-C technique are to be trusted. The following technique is useful because it allows this current to be determined very accurately.

We will explain the device behavior with the aid of the diagrams in Fig. 1, showing the capacitance–time (C–t), capacitance–voltage (C–V_G), and charge–voltage (Q–V_G) plots. Q–V_G plots are rarely shown, but can be very beneficial to understand the behavior of pulsed MOS capacitors. Fig. 1(a) shows

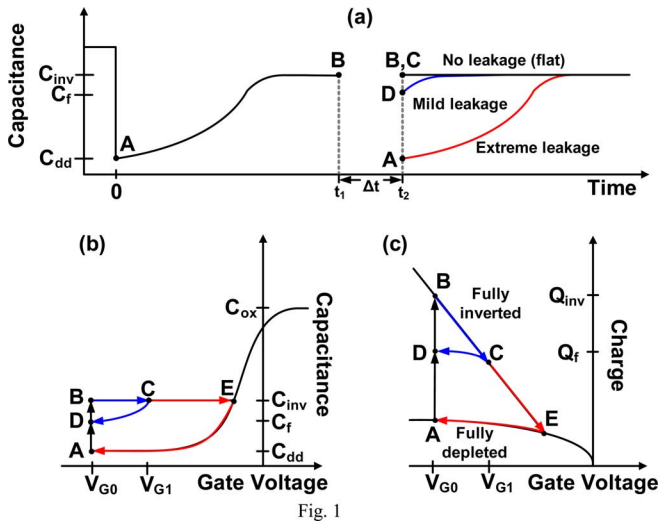

Fig. 1

Fig. 1. Qualitative plots of (a) *C–t*, (b) $C - V_G$, and (c) $Q - V_G$ described in the text for an *n*-type substrate.

a *C–t* plot of a pulsed MOS-C after a depleting gate voltage pulse is applied at $t = 0$. The capacitance drops rapidly to its deep-depleted capacitance, $C_{\rm dd}$, at point A and, subsequently, recovers to its inversion capacitance, $C_{\rm inv}$, at point B, at $t = t_1$, as a result of the electron–hole pair (ehp) generation. This recovery takes place for a constant gate voltage V_{G0} since the probe contacts the gate during this time. On the $Q - V_G$ plot, the semiconductor charge is initially all depletion charge at A, which changes to B when the inversion layer has fully formed. The negative gate charge is compensated by holes in the inversion layer and positively charged donors in the space–charge region. At $t = t_1$, the probe is lifted off the gate contact for time Δt and reapplied at $t = t_2$.

Now that the probe is no longer forcing a constant gate voltage, two things may happen. First: there is *no* oxide leakage current and the electrons originally on the gate will remain there, the holes in the inversion layer remain at the semiconductor–oxide interface, and the gate voltage remains unchanged. Point B remains unchanged and is shown in Fig. 1(a) as "no leakage." In the second case, there *is* an oxide leakage current. When the probe is lifted at point t_1, some of the holes in the inversion layer drift through the oxide to the gate, where they neutralize electrons in the negatively charged gate metal. Since the device is still in inversion, there is no ehp generation, and the surface potential is pinned to a value close to twice the Fermi potential. However, the leaked inversion charge leads to a gate voltage change to V_{G1}. The inversion charge decreases from B to C, but the capacitance remains at $C_{\rm inv}$, and all plots in Fig. 1 will be at point C.

When the probe is reapplied to the gate, the gate voltage returns to its original value V_{G0}. The device is driven to point D (mild leakage) and the leaky device is in partial deep depletion at capacitance C_f. Now that some of the inversion holes are lost by leaking through the oxide, those holes must be generated again. With time, ehp generation returns the device to B. For high oxide leakage current, point B goes to the "no inversion charge" point E (extreme leakage) instead of C. Reapplying the gate voltage drives the device to point A and thermal generation returns it to point B. These figures show that when the gate voltage is reapplied at the end of the "probe off the gate" period Δt, the capacitance depends on the oxide leakage current. Hence, a measure of that capacitance is an indirect measure of the oxide leakage current.

The charge that leaks through the oxide during the time Δt can be quantified. The change in charge between points A and B is given by $\Delta Q = Q_f - Q_{\rm inv}$. The charge can be found by relating the capacitance to the inversion/deep-depletion charge, Q_p, with the equation [11]

$$C = \frac{C_{\rm ox}}{\sqrt{1 + \frac{2}{V_0}\left(V_G' + \frac{Q_p}{C_{\rm ox}}\right)}} \tag{1}$$

where $V_0 = -qK_s\varepsilon_0 N_D / C_{\rm ox}^2$ and $V_G' = V_G - V_{\rm FB}$. All the equations are derived for an n-type (p-channel) MOS-C in order to remain consistent with the experimental data presented in the next section. Equation (1) was originally derived using the delta-depletion approximation to describe the relation between capacitance and inversion layer charge in a nonequilibrium MOS-C, and is sufficiently accurate for our calculations. At points C, D, and E in Fig. 1, C_f is the final capacitance; we will denote the corresponding charge as Q_f. Since the capacitance is known, we need to solve (1) for the inversion charge as a function of capacitance. Thus, the charge at points C, D, and E in Fig. 1 is given by

$$Q_f = C_{\rm ox}\left\{\frac{V_0}{2}\left[\left(\frac{C_{\rm ox}}{C_f}\right)^2 - 1\right] - V_{G'}\right\}. \tag{2}$$

The inversion charge is simply obtained by substituting the inversion capacitance in (2). Thus, the leaked charge is just the difference between the inversion charge and the charge at the point when the probe is reapplied, which simplifies to

$$\Delta Q = \frac{V_0 C_{\rm ox}^3}{2}\left(\frac{1}{C_f^2} - \frac{1}{C_{\rm inv}^2}\right) \tag{3}$$

where ΔQ represents the charge that leaked through the oxide during the time the probe was disconnected. At this point, the leakage current can be estimated simply by dividing the charge by the "noncontact" time Δt. This implies that the current is constant-–an unrealistic assumption. Thus, we shall proceed with a more formal derivation assuming an arbitrary form for the leakage current, and solve for the necessary parameters. We begin with the equation that governs the capacitance and voltage of an MOS-C during the pulsed measurement [11]

$$\frac{dV_G}{dt} = -\frac{1}{C_{\rm ox}}\frac{dQ_p}{dt} + \frac{qK_s\varepsilon_o N_D}{C^3}\frac{dC}{dt}. \tag{4}$$

In our situation, the capacitance clearly remains at the inversion value when the probe is lifted. Furthermore, the only change in charge must be due to leakage current. Thus, (4) reduces to

$$\frac{dV_G}{dt} = -\frac{1}{C_{\rm ox}}\frac{dQ_p}{dt} = -\frac{1}{C_{\rm ox}}J_{\rm leak}\left(V_G\right) \tag{5}$$

where $J_{\rm leak}\,(V_G)$ is negative. Equation (5) states that leakage current is directly proportional to the rate of gate voltage change. To solve (5), we first assume the current to be constant, giving

$$\frac{dV_G}{dt} = -\frac{1}{C_{\rm ox}} J_{\rm leak}\,(V_G) = -\frac{J_0}{C_{\rm ox}}. \tag{6}$$

Integrating both sides and solving for the constant current density, J_0, yields

$$J_0 = C_{\rm ox}\frac{V_{Gf} - V_{Gi}}{t_f - t_i} = \frac{C_{\rm ox}\Delta V}{\Delta t} = \frac{\Delta Q}{\Delta t} \tag{7}$$

where ΔQ is given by (3).

A more realistic case is an ohmic oxide leakage current. To simplify the analysis, we consider a constant oxide electric field, which in inversion is given by

$$E_{\rm ox} = \frac{V_G' - 2\phi_F}{t_{\rm ox}}. \tag{8}$$

Thus, the form of the leakage current is

$$J_{\rm leak}\,(V_G) = \sigma_{\rm ox} E_{\rm ox}\,(V_G) = \sigma_{\rm ox}\frac{V_G' - 2\phi_F}{t_{\rm ox}} \tag{9}$$

where we have introduced the effective conductivity in the insulator, $\sigma_{\rm ox}$. Equation (5) becomes

$$\frac{dV_G}{dt} = -\frac{1}{C_{\rm ox}}\sigma_{\rm ox}\frac{V_G' - 2\phi_F}{t_{\rm ox}} \tag{10}$$

Integrating (10) and solving for the conductivity yields

$$\sigma_{\rm ox} = \frac{\varepsilon_{\rm ox}}{\Delta t}\ln\left(\frac{V_{Gi}' - 2\phi_F}{V_{Gf}' - 2\phi_F}\right). \tag{11}$$

In this case, we need to know the actual voltages, not just the difference in charge. V_{Gi}' is the gate voltage corrected for $V_{\rm FB}$, and V_{Gf}' can be found from the leaked charge as

$$V_{Gf}' = V_{Gi}' - \Delta Q/C_{\rm ox} \tag{12}$$

where ΔQ is given by (3). This voltage is not actually measured because the probe remains at a constant voltage when it contacts the gate again. If one were to attempt to measure this voltage, the finite input impedance of the voltmeter would immediately discharge the device.

A more complex situation is the case when the leakage current depends exponentially on the oxide field, as for the Fowler–Nordheim (F–N) tunneling. The expression for the F–N leakage for current density of an n-type MOS-C is [12]

$$J_{\rm leak} = -AE_{\rm ox}^2\exp\left(\frac{-B}{|E_{\rm ox}|}\right) \tag{13}$$

where A and B are constants that depend on the barrier height Φ_B, and the effective mass in the insulator, $m_{\rm ox}$. Using (8) in (13), (5) becomes

$$C_{\rm ox}\frac{dV_G}{dt} = A\left(\frac{V_G' - 2\phi_F}{t_{\rm ox}}\right)^2\exp\left(\frac{-Bt_{\rm ox}}{|V_G' - 2\phi_F|}\right). \tag{14}$$

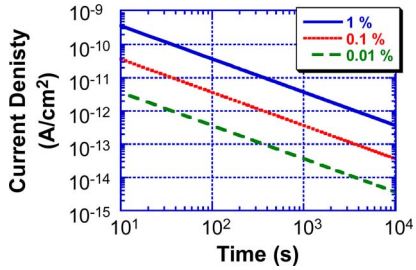

Fig. 2. Plot of minimum detectable gate current density versus measurement time. Typical device parameters were used, and it was assumed that it is possible to resolve 1% (solid), 0.1% (dashed), and 0.01% (dotted) differences in capacitance between sequential time samples.

Integration of (14) yields

$$\frac{t_{\rm ox}^2 C_{\rm ox}}{A}\int_{V_{Gi}}^{V_{Gf}}(V_G' - 2\phi_F)^{-2}\exp\left(\frac{Bt_{\rm ox}}{|V_G' - 2\phi_F|}\right)dV_G' = \int_{t_i}^{t_f} dt. \tag{15}$$

It is possible to expand and solve (15) in terms of special functions. However, since the introduction of special functions requires a numerical solution, it is preferred to simply evaluate (15). Thus, using the technique just illustrated, any relationship between oxide leakage current and electric field can be substituted, and a solution derived.

A few points should be made about the accuracy of this technique. First, the lost inversion charge is always given by (3), *regardless of the form of the current-electric field relationship*. The assumption of a mathematical form for this relationship is only required in order to derive an expression for the time dependence of this charge loss. Of course, it is helpful if the relationship is known from current–voltage measurements.

In addition, inaccuracies arise if the sampling times are not sufficiently fast, especially for high generation current. This is because a high generation current may significantly raise the capacitance after the probe has been reapplied, but before the first capacitance sample is taken. This can be avoided by assuring the sampling time to be sufficiently long to distinguish small changes in capacitance over each step. For example, in one of our typical devices, generation causes the capacitance to rise about 1% in 1 s. Thus, a sampling rate of 1 Hz allows us to distinguish a 1% change in the capacitance. This limit can be easily extended by triggering the capacitance meter to sample immediately when the probe is replaced.

The lower detection limit is determined by the time available for the measurement. Fig. 2 plots the gate current versus measurement time for a sampling rate consistent with 1%, 0.1%, and 0.01% changes in capacitance, showing that current densities of the order of $10\,{\rm fA/cm^2}$ can be determined after waiting 10^4 s. The measurements should be made in the dark as optical ehp generation affects the measurements. The *maximum* current which can be measured is limited by the charge in the inversion layer. Clearly, once the entire inversion layer has been depleted, the final capacitance ceases to depend on time. This is easy to recognize, as the final capacitance will be the same as the deep-depletion capacitance [see the "Extreme leakage" case in Fig. 1(a)].

Next, it is useful to study the effect of the gate leakage current on the recovery of the pulsed MOS-C from deep depletion. This has been discussed by Xu *et al.* for the case of the Fowler–Nordheim leakage current [13]; here, a more general theory is developed. During the recovery from deep depletion, the gate voltage is constant, which makes the left-hand side of (4) zero

$$0 = -\frac{1}{C_{\rm ox}}\frac{dQ_p}{dt} + \frac{qK_s\varepsilon_o N_D}{C^3}\frac{dC}{dt}. \tag{16}$$

In general, the leakage current depends on the oxide electric field. When considering this, the rate of change of the charge is given by [14]

$$\frac{dQ_p}{dt} = qn_i\frac{W - W_F}{\tau_{g,\rm eff}} + qn_i s_{g,\rm eff} + J_{\rm leak}\left(W\right) \tag{17}$$

where $J_{\rm leak}\left(W\right)$ is negative. The relationship between the scr width and capacitance is

$$W = \frac{K_s\varepsilon_{\rm o}\left(C_{\rm ox} - C\right)}{CC_{\rm ox}} \tag{18}$$

which allows us to combine (16)–(18) as

$$\frac{C_{\rm ox}K_s\varepsilon_{\rm o}N_D}{C^3}\frac{dC}{dt} = \frac{K_s\varepsilon_{\rm o}n_i}{\tau_{g,\rm eff}C_{\rm inv}}\left(\frac{C_{\rm inv}}{C} - 1\right) + n_i s_{g,\rm eff} + \frac{J_{\rm leak}\left(C\right)}{q}. \tag{19}$$

Thus, (19) provides a function that relates the capacitance relaxation to time. However, in order to write the oxide leakage current as a function of capacitance, we must consider the electric field's relationship to the capacitance during the transient. The oxide electric field as a function of gate voltage and surface potential is

$$E_{\rm ox}\left(W\right) = \frac{V_G' - \phi_s\left(W\right)}{t_{\rm ox}} \tag{20}$$

where the surface potential as a function of the scr width is given by

$$\phi_s\left(W\right) = -\frac{qN_D W^2}{2K_s\varepsilon_{\rm o}}. \tag{21}$$

Therefore, we can use (18), (20), and (21) to write the electric field as a function of the capacitance during the relaxation

$$E_{\rm ox}\left(C\right) = \frac{V_G'}{t_{\rm ox}} + \frac{qN_D K_s\varepsilon_{\rm o}}{2t_{\rm ox}}\left(\frac{1}{C} - \frac{1}{C_{\rm ox}}\right)^2. \tag{22}$$

For example, for an ohmic oxide current density of the form $J_{\rm leak}\left(V_G\right) = \sigma_{\rm ox}E_{\rm ox}\left(C\right)$, (19) becomes

$$\frac{C_{\rm ox}K_s\varepsilon_{\rm o}N_D}{C^3}\frac{dC}{dt} = \frac{K_s\varepsilon_{\rm o}n_i}{\tau_{g,\rm eff}C_{\rm inv}}\left(\frac{C_{\rm inv}}{C} - 1\right) + n_i s_{g,\rm eff} + \frac{\sigma_{\rm ox}}{qt_{\rm ox}}\left[V_G' + \frac{qN_D K_s\varepsilon_{\rm o}}{2}\left(\frac{1}{C} - \frac{1}{C_{\rm ox}}\right)^2\right]. \tag{23}$$

Although (23) can be simplified and integrated to find an analytical solution, the form of the solution is awkward. It is, thus, simpler to evaluate this equation numerically, which is done

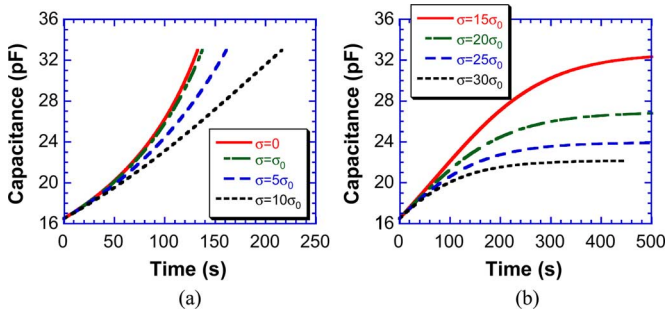

Fig. 3. Capacitance transients with ohmic oxide leakage current for several values of oxide conductivities (a) recovery is possible and (b) recovery does not occur.

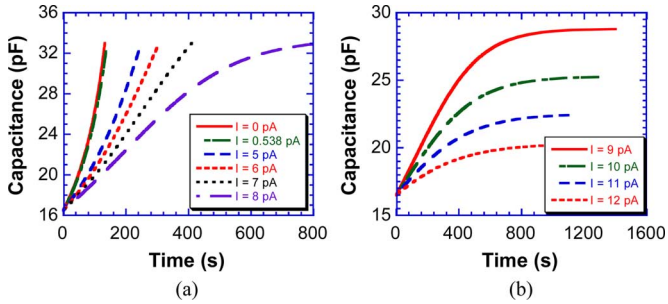

Fig. 4. Capacitance transients for several values of constant leakage current (a) recovery is possible and (b) recovery does not occur.

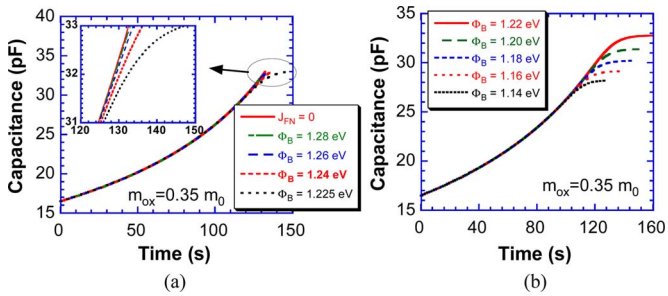

Fig. 5. Capacitance transients for Fowler–Nordheim tunneling current as a function of Φ_B (a) recovery is possible and (b) recovery does not occur.

in Fig. 3 for several values of $\sigma_{\rm ox}$. In addition, a solution is found where a constant leakage current is present (Fig. 4), as well as for the case of the F–N tunneling (Fig. 5). An interesting result of Figs. 3–5 is that while oxide leakage current has a significant effect on the recovery time for a constant or ohmic leakage current, an F–N leakage current does not significantly alter the behavior until a specific capacitance is reached. If the F–N tunneling is causing a significant oxide leakage current, full recovery becomes impossible very quickly. Fig. 5(a) shows the narrow range of barrier heights where the F–N tunneling current affects the *C–t* response, but recovery is still possible; Fig. 5(b) demonstrates the case where recovery is not possible.

Of course, the primary purpose of the pulsed MOS-C measurement is to determine the generation lifetime. This is

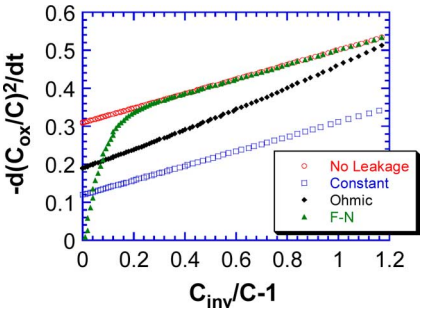

Fig. 6. Effects of several forms of leakage current on the Zerbst plot.

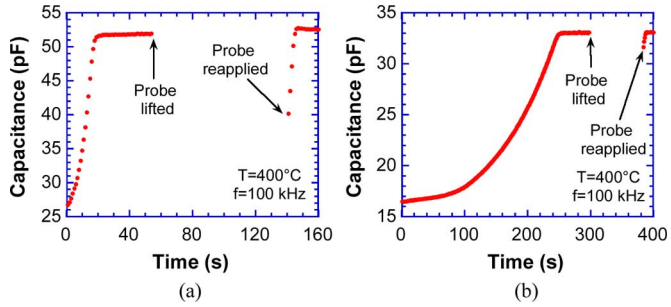

Fig. 7. Experimental C–t curve followed by a probe-lift test for an oxide with (a) high and (b) moderate leakage current. In (b), the capacitance drops when the probe is lifted at 300 s (not shown) due to gate oxide current and when the probe is reapplied at 380 s, the capacitance quickly recovers.

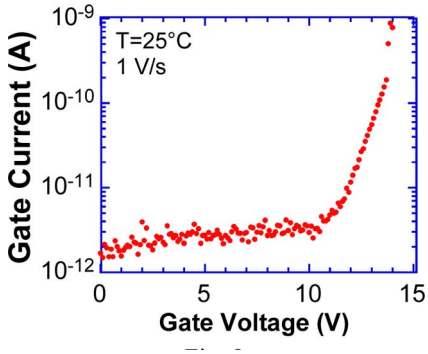

Fig. 8. Gate current–gate voltage characteristic for the device in Fig. 7(b).

accomplished by rewriting (19) as

$$-\frac{d}{dt}\left(\frac{C_{\rm ox}}{C}\right)^2 = \frac{2n_i C_{\rm ox}}{\tau_{g,\rm eff} N_D C_{\rm inv}}\left(\frac{C_{\rm inv}}{C}-1\right) + \frac{2K_{\rm ox} n_i s_{g,\rm eff}}{K_S t_{\rm ox} N_D} + \frac{2K_{\rm ox} J_{\rm leak}\,(C)}{qK_S t_{\rm ox} N_D}. \quad (24)$$

If the leakage current term is ignored, a plot of $-d/dt(C_{\rm ox}/C)^2$ versus $(C_{\rm inv}/C-1)$ has a slope of $2n_i C_{\rm ox}/N_D C_{\rm inv}\tau_{g,\rm eff}$ and an intercept of $2n_i K_{\rm ox} s_{g,\rm eff}/K_S t_{\rm ox} N_D$ – a standard Zerbst plot. With a constant leakage current, the slope is not changed, but the intercept becomes $2K_{\rm ox}/K_S t_{\rm ox} N_D\,(n_i s_{g,\rm eff} + J_{\rm leak}/q)$. A constant leakage current simply offsets surface generation. However, in the case of an ohmic leakage current, the slope is modified to

$$\frac{2n_i C_{\rm ox}}{\tau_{g,\rm eff} N_D C_{\rm inv}} + \frac{2\sigma_0}{t_{\rm ox} C_{\rm inv}}\left(\frac{C_{\rm ox}}{C}-1\right) \quad (25)$$

which renders the Zerbst plot difficult to interpret. This becomes even more complicated for the F–N leakage current. However, the exponential dependence of current on oxide electric field causes the effect of the F–N current on the C–t measurements to be experienced only when the current exceeds a certain value. It can, therefore, be assumed that the slope of the Zerbst plot is unaffected until this onset a point, which is clearly identifiable. Fig. 6 illustrates each of these cases on a sample Zerbst plot, showing the effect of various currents on the slope and intercept.

III. Experimental Results

Our generation lifetime and oxide leakage measurements were made on 4H-SiC/SiO_2 MOS capacitors. The aforementioned technique has been very useful, as these devices typically have higher oxide leakage currents than silicon devices. This can be partly attributed to the fact that we measure the MOS-C at 400 °C to raise the intrinsic carrier concentration (n_i) to achieve a reasonably fast recovery time. For example, for a 4H-SiC MOS-C with a 1-μs lifetime and $N_D = 10^{16}$ cm^{-3}, the recovery time, approximately given by $10N_D\tau_{g,\rm eff}/n_i$ [11], is 5 min at 400 °C with $n_i \approx 1.7 \times 10^8$ cm^{-3} [15]. Clearly, it is necessary to make these measurements at a high temperature to obtain reasonable recovery times. Unfortunately, the gate oxide leakage currents are much higher than at room temperature.

The MOS capacitors were fabricated on Dow Corning 4H-SiC n-type, research-grade wafers with a 20-μm epi-layer doped to about 6×10^{15} cm^{-3}. The wafers were oxidized for 8 h at 1150 °C for an approximately 67-nm thick oxide. A 2-h NO passivation was used to minimize the interface state density ($D_{\rm it}$). Details of the oxidation process can be found in [16].

The probe-lift technique is used after each test to verify the accuracy of our lifetime measurements. If it results in a current much higher than the device generation current, then the generation lifetimes extracted from the Zerbst plot are inaccurate. An example of the data obtained from this procedure is shown in Fig. 7(a) for a device with a very high leakage current and in Fig. 7(b) for a device with a more moderate leakage current compared to the generation current. The curves in Fig. 7 are similar to those in Fig. 1(a). As an example, we will consider the data in Fig. 7(b), since this case yields a more accurate result (as elaborated on later). A constant leakage current calculated using (7) gives 538 fA. If the ohmic assumption is used, then from (11), the effective oxide conductivity is about $\sigma_{\rm ox} = 10^{-16}$ S/cm, giving an initial current of 545 fA, which falls to 530 fA immediately before the probe contacts the gate.

For the F–N tunneling current, it is necessary to assume either an oxide effective mass $m_{\rm ox}$, or a barrier height, $\Phi_{B,\rm eff}$, and use the other as a fitting parameter. We use $m_{\rm ox} = 0.35\,m_0$ as given by Chanana *et al.* for holes in SiO_2 on 4H-SiC (m_0 denotes the free electron mass) [17]. Substituting this value in (15) leads to an effective barrier height of 1.267 eV, giving the F–N constants $A = 3.48 \times 10^{-6}$ A/V^2, and $B = 5.76 \times 10^7$ V/cm. Although this value of $\Phi_{B,\rm eff}$ is low, it has been shown that it is significantly lowered by temperature in 4H-SiC [18]. In addition, the room temperature $I-V$ plot for this device in Fig. 8 appears

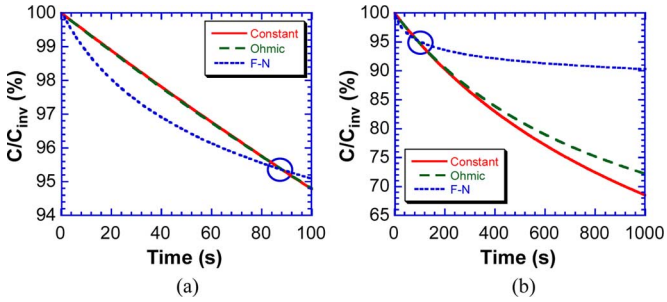

Fig. 9. Normalized capacitance versus time due to various forms of oxide leakage current corresponding to the data in Fig. 7, for a maximum duration of (a) 100 s and (b) 1000 s.

to exhibit the behavior characteristic of the F–N tunneling before breakdown. However, the rather low-breakdown electric field ($E_{\rm ox} \approx 2$ MV/cm) suggests that defects may significantly degrade the SiC/SiO_2 interface and the oxide of this device.

At low temperatures, when generation is insignificant, the procedure can be modified by using light to generate an inversion layer, which has the added advantage that the accuracy does not depend on the sampling rate, because once the probe is reapplied to the gate in the dark, if generation is negligible, the capacitance is nearly static. Thus, the accuracy is only dependent on the resolution of the meter. In this way, a capacitance drop corresponding to a constant current of 0.8 fA has been measured.

In order to verify the accuracy of this technique, the current–time ($I - t$) measurements were made similar to the capacitance–time measurements. The device was pulsed into deep depletion and the current was recorded as the inversion layer formed. The current is initially mainly due to thermal generation. However, once the inversion layer has formed, the current that is measured is the gate oxide leakage current. We have found that the current obtained from $I - t$ measurements closely matches the current obtained from the probe-lift technique with the assumption of a constant current, as long as the capacitance has not deviated much from its inversion value. Thus, to obtain the most accurate results, the measurement procedure should be timed so that the final capacitance differs less than about 10% from its original value.

Two considerations illustrate why inaccurate results occur when the capacitance has departed significantly from inversion. The first is quite simple: in the case where the final capacitance is approximately at the original deep depletion value, the measured data are invalid, because after the device has been fully depleted due to leakage, the capacitance ceases to depend on time. The second consideration is more subtle. When the final capacitance is still very close to its original inversion value, the electric field across the oxide has hardly changed during the time of the probe lift. If this happens, the relationship between the leakage current and the capacitance is not very important. As the oxide electric field decreases due to the loss of inversion charge, the current decreases. Thus, the dependence of the leakage current on the oxide electric field becomes increasingly important, especially if the current depends exponentially on the electric field.

This point is further clarified by Fig. 9. Fig. 9(a) shows the capacitance–time behavior during the probe-lift time for each of the three assumed forms of current and the experimental results obtained from Fig. 7(b). It is nearly impossible to experimentally observe this behavior, as any perturbation of the charge on the gate will significantly alter the measurement. Fig. 9(a) clearly shows that the constant and ohmic curves are nearly identical, indicating that the assumed current–electric field relationship is inconsequential. Even the exponential dependence of the F–N current is reasonably similar to the other two. However, if the final capacitance has recovered significantly from its initial value, a different behavior emerges. As illustrated in Fig. 9(b), which is an extension of Fig. 9(a) to $t = 1000$ s, when the final capacitance deviates significantly from the initial inversion value, the assumed current–field relationship begins to play a significant role—especially if it is exponential. Therefore, as long as the capacitance does not deviate significantly from its inversion value, accurate results can be obtained using this technique even if the assumed form of the current is not correct. Of course, as stated earlier, if one only wants to know the leaked charge during the time of the measurement, (3) can be used without making any assumptions about the form of the current–oxide electric field relationship.

IV. Conclusion

A novel MOS-C technique has been presented, which allows the characterization of extremely low oxide leakage currents. In this method, the probe is lifted off the gate of an MOS capacitor biased into strong inversion. As some of the inversion charge leaks through the gate oxide to the floating gate, the capacitance is reduced. This reduced capacitance, measured when the probe touches the gate again, is analyzed and used to extract the oxide leakage current. The magnitude of the leakage current that can be measured is limited only by the time required by the measurement. Equations have been derived to solve for the leakage current parameters for several current–oxide electric field relationships. Furthermore, we have modeled the effects of leakage current on the pulsed MOS-C measurements and the resulting Zerbst plots, showing that such leakage currents can influence the extraction of generation lifetime.

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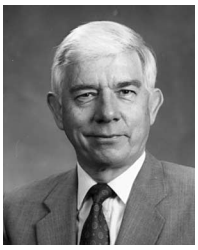

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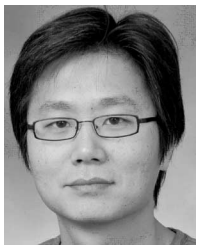

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